DESCRIPTION

THREE-PHASE PWM-SIGNAL GENERATING APPARATUS

5   TECHNICAL FIELD

[0001]

     The present invention relates to a three-phase pulse-
width-modulation (PWM)-signal generating apparatus that
generates a three-phase PWM signal for defining a switching

10   mode set by a semiconductor switching element in a three-
phase voltage inverter.

BACKGROUND ART

[0002]

15   A three-phase voltage inverter is used for an inverter
for, for example, an inverter for controlling to drive a
motor of a refrigeration air conditioning apparatus. To
facilitate understanding of the present invention, a
constitution and an operation of a conventional inverter

20   are explained below with reference to Figs. 36 to 42.

[0003]

     Fig. 36 is a block diagram of an example of the
conventional inverter. The conventional inverter shown in
Fig. 36 includes an inverter main circuit 1 and an inverter

25   control unit 2 that generates a three-phase PWM signal that
is a drive signal for a semiconductor switching element
included in the inverter main circuit 1. In other words,
the present invention relates to an improvement of the
inverter control unit 2.

30   [0004]

     The inverter main circuit 1 is a well-known circuit
including a DC power supply 3 that gives a bus voltage Vdc,
three sets of semiconductor switching elements (5a, 5b),

(5c, 5d), and (5e, 5f) that are connected in series between a DC bus 4a connected to a positive pole of the DC power supply 3 and a DC bus 4b connected to a negative pole of the DC power supply 3, and flywheel diodes 6a to 6f that are connected in series to the respective semiconductor switching elements. A motor 7 is connected to respective DC connection terminals of the three sets of semiconductor switching elements (5a, 5b), (5c, 5d), and (5e, 5f).
[0005]

A DC current detecting unit 9, which detects a DC bus current Idc used in the inverter control unit 2, is provided in, for example, the DC bus 4b. The DC current detecting unit 9 includes a detection element (a resistor, a current transformer, etc.) inserted in the DC bus 4b and an amplifier that amplifies a both-end voltage of the detection element (the resistor) or an output voltage of the detection element (the current transformer). The DC current detecting unit 9 converts an output voltage of this amplifier into an electric current to obtain a DC bus current Idc.
[0006]

The inverter control unit 2 includes a phase-current discriminating unit 11 that discriminates phase currents Iu, Iv, and Iw from the DC bus current Idc inputted from the DC current detecting unit 9, a unit 12 that calculates an excitation current and a torque current for calculating an excitation current Iγ (a γ axis current) and a torque current Iδ (a δ axis current) from the phase currents Iu, Iv, and Iw, a voltage-command-vector calculating unit 13 that calculates a voltage command vector V* used in the next control from the excitation current Iγ and the torque current Iδ, a PWM-signal creating unit 14 that produces

conducting time signals Tup, Tun, Tvp, Tvn, Twp, and Twn, which are three-phase PWM signals during one carrier period, from the voltage command vector V*, and a PWM-signal generating unit 15 that generates driving signals Up, Un,

5   Vp, Vn, Wp, and Wn, which are three-phase PWM signals applied to the semiconductor switching elements 5a to 5f, from the conducting time signals Tup, Tun, Tvp, Tvn, Twp, and Twn. Note that a subscript "p" means a positive pole side and a subscript "n" means a negative pole side.

10   [0007]

An operation of the inverter control unit 2 is explained. Among the semiconductor switching elements 5a to 5f of the inverter main circuit 1, the semiconductor switching elements 5a, 5c, and 5e connected to the DC bus

15   4a on the positive pole side perform an ON operation or the semiconductor switching elements 5b, 5d, and 5f connected to the DC bus 4b on the negative pole side perform an ON operation. Since there are the semiconductor switching elements for three phases, eight ($2^3=8$) kinds of switching

20   patterns or switching modes are present in total. These are states of output to the motor 7.
[0008]

As state representation of the semiconductor switching elements, an ON operation state of the semiconductor

25   switching elements is represented as a logical value 1 and an OFF operation state of the semiconductor switching elements is represented as a logical value 0. Eight kinds of states of output to the motor 7 are associated with eight kinds of voltage vectors (basic voltage vectors) of

30   V0 to V7 as described below. Among these eight kinds of voltage vectors, V1 to V6 are voltage vectors corresponding to six switching modes having vector lengths and the remaining V0 and V7 are voltage vectors corresponding to

two switching modes not having vector lengths. The voltage
vectors V0 and V7 are specifically referred to as "zero
vectors". The voltage vectors V1 to V6 are often referred
to as "basic voltage vectors" to be distinguished from the
5   "zero vectors".
[0009]

       A correspondence relation among the voltage vectors V1
to V6 is represented by logical states of the switching
elements connected to the DC bus 4a, namely, a logical
10   state of W-phase positive pole side switching elements, a
logical state of V-phase positive pole side switching
elements, and a logical state of U-phase positive pole side
switching elements. The logical states(0, 0, 1) correspond
to the voltage vector V1, the logical states (0, 1, 0)
15   correspond to the voltage vector V2, the logical states (0,
1, 1) correspond to the voltage vector V3, the logical
states (1, 0, 0) correspond to the voltage vector V4, the
logical states (1, 0, 1) correspond to the voltage vector
V5, and the logical states (1, 1, 0) correspond to the
20   voltage vector V6.
[0010]

       A correspondence relation between the two zero vectors
V0 and V7 is represented by logical states of the switching
elements connected to the DC bus 4a, namely, a logical
25   state of W-phase positive pole side switching elements, a
logical state of V-phase positive pole side switching
elements, and a logical state of U-phase positive pole side
switching elements. The logical state (0, 0, 0)
corresponds to the zero vector V0 and the logical state (1,
30   1, 1) corresponds to the zero vector V7.
[0011]

       While the six voltage vectors V1 to V6 are produced,
an electric current flowing to a winding of the motor 7

flows to the DC buses 4a and 4b. Thus, it is possible to detect the electric current with the DC current detecting unit 9 and observe the electric current as the DC bus current Idc. On the other hand, while the zero vectors V0 and V7 are produced, it is impossible to observe the electric current as the DC bus current Idc.

[0012]

Fig. 37 is a table of a relation between eight kinds of basic voltage vectors, switching modes corresponding to the basic voltage vectors, and phase currents that can be observed as a DC bus current Idc. As shown in Fig. 37, it is impossible to observe a phase current in the zero vectors V0 and V7. However, a phase current is observed as "Iu (U-phase current)" in the voltage vector V1, observed as "Iv (V-phase current)" in the voltage vector V2, observed as "-Iw (W-phase current)" in the voltage vector V3, observed as "Iw" in the voltage vector V4, observed as "-Iv" in the voltage vector V5, and observed as "-Iu" in the voltage vector V6.

[0013]

To rotate the motor 7 smoothly, it is necessary to obtain a magnetic flux corresponding to a desired voltage and a desired frequency. This can be realized by combining the eight kinds of voltage vectors appropriately. Fig. 38 is a diagram for explaining a phase relation between the basic voltage vectors and a relation between the inverter rotation angle and a voltage command vector. In Fig. 38, when an inverter rotation direction is clockwise, the six voltage vectors V1 to V6 are arranged on a phase plane in an order of V1, V3, V2, V6, V4, and V5 clockwise at a phase difference of 60 degrees. The two zero vectors V0 and V7 are shown in an origin position.

[0014]

In Fig. 38, an inverter rotation angle θ having a direction of the voltage vector V1 (U-phase) as an initial phase gives a phase of a voltage command vector V*. A phase angle between one of the six voltage vectors, which are produced in the inverter rotation direction, and the voltage command vector V* is referred to as a spatial vector rotation angle θ*. Note that an angle range of the spatial vector rotation angle θ* is 0 degree ≤ θ* < 60 degrees.

[0015]

Production ratios of the respective voltage vectors depend on a percentage modulation that is a ratio of an output voltage to a bus voltage. Production times of the respective voltage vectors depend on the voltage command vector V* and the spatial vector rotation angle θ*. Thus, the phase-current discriminating unit 11 calculates the phase currents Iu, Iv, and Iw from the DC bus current Idc in accordance with the table shown in Fig. 37 while the respective voltage vectors are produced.

[0016]

Subsequently, the unit 12 for calculating an excitation current and a torque current converts the phase currents Iu, Iv, and Iw calculated by the phase-current discriminating unit 11 into an excitation current Iγ (a γ axis current) and a torque current Iδ (a δ axis current) using, for example, a three-phase to two-phase conversion matrix $[C_1]$ indicated by Equation (1) and a rotation matrix $[C_2]$ indicated by Equation (2). Note that, in Equation (2), θ indicates an inverter rotation angle, and a rotation direction is clockwise.

[0017]

$$[C_1] = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \qquad (1)$$

[0018]

$$[C_2] = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \qquad (2)$$

[0019]

5   A coordinate system, on which the unit 12 for calculating an excitation current and a torque current is based, is a γ-δ axis rather than a d-q axis. This point is explained below. An N pole side on a rotor of the motor 7 is set as a d axis and a phase advanced 90 degrees (an

10   electrical angle) in a rotation direction is set as a q axis. When a sensor for detecting a rotor position like a pulse encoder is not used for driving of a synchronous motor, the inverter control unit 2 cannot grasp a d-q axis coordinate of the rotor accurately. Actually, the inverter

15   control unit 2 performs control with a coordinate system shifted by a phase difference Δθ from the d-q axis coordinate system. This coordinate system shifted by the phase difference Δθ is generally referred to as a γ-δ axis coordinate. It is a practice to use this γ-δ axis

20   coordinate. This also applies in this specification.
      [0020]
      The voltage-command-vector calculating unit 13 performs various kinds of vector control operation including speed control based on the excitation current Iγ

25   (the γ axis current) and the torque current Iδ (the δ axis current) calculated by the unit 12 for calculating an excitation current and a torque current. The voltage-command-vector calculating unit 13 calculates a magnitude

and a phase of the voltage command vector V* used for the next control. This phase angle is the inverter rotation angle θ as described above.

[0021]

The PWM-signal creating unit 14 produces conducting time signals Tup, Tun, Tvp, Tvn, Twp, and Twn based on the voltage command vector V* according to various systems described later. Consequently, the PWM-signal generating unit 15 generates three-phase PWM signals Up, Un, Vp, Vn, Wp, Wn, which are driving signals applied to the semiconductor switching elements 5a to 5f, from the conducting time signals Tup, Tun, Tvp, Tvn, Twp, and Twn and controls the semiconductor switching elements 5a to 5f. As a result, the motor 7 is driven.

[0022]

As a system for generating a PWM signal in the PWM-signal creating unit 14, conventionally, two systems have been mainly used. One system is a system for generating a PWM signal using four kinds of basic voltage vectors in total, namely, two kinds of basic voltage vectors with a phase difference of 60 degrees and two kinds of zero vectors not having a magnitude that are obtained by switching only one phase of switching states of the two kinds of basic voltage vectors (hereinafter referred to as "three-phase modulation system"). The other system is a system for generating a PWM signal using three kinds of basic voltage vectors in total, namely, two kinds of basic voltage vectors with a phase difference of 60 degrees and one of the two kinds of zero vectors not having a magnitude (hereinafter referred to as "two-phase modulation system").

[0023]

Specifically, this is a method of, by decomposing the voltage command vector V* from the voltage-command-vector

calculating unit 13 in directions of two basic voltage vectors corresponding thereto, generating production time ratios of the respective basic voltage vectors and calculating conducting times (or non-conducting times) of the respective semiconductor switching elements during one carrier period. This system has problems described below.

[0024]

A ratio of an output voltage to a DC bus voltage is referred to as a percentage modulation. In the three-phase modulation system or the two-phase modulation system, when the percentage modulation is low, production time ratios of both the two kinds of basic voltage vectors having a magnitude and a phase difference of 60 degrees decreases and a holding time width of a switching mode is narrowed. Even if the percentage modulation is high to some extent, when the voltage command vector V* is close to one of the basic voltage vectors, a production time ratio of the other basic voltage vector distant from the voltage command vector V* decreases and a holding time width of a switching mode is narrowed.

[0025]

In these two cases, there is a problem in that, in a production section of a basic voltage vector with a short holding time width of a switching mode, since a sufficient DC current detection time cannot be secured and current detection cannot be performed correctly, controllability is deteriorated significantly.

[0026]

Thus, in recent years, to secure a holding time width of a switching mode in the cases described above, a system for generating a PWM signal with a switching pattern different from the three-phase system and the two-phase system (hereinafter referred to as "extended PWM system")

has been proposed (e.g., patent document 1).

[0027]

The patent document 1 discloses a three-phase PWM voltage generating circuit that generates a three-phase PWM voltage signal using three kinds of basic voltage vectors in total, namely, two kinds of basic voltage vectors with a phase difference of 120 degrees and a zero vector not having a magnitude that is obtained by switching only one phase of switching states of these basic voltage vectors. The patent document 1 also discloses a three-phase PWM voltage generating circuit that generates a three-phase PWM voltage signal using three-kinds of basic voltage vector having phase differences of 60 degrees, respectively.

[0028]

In this extended PWM system, the conducting time signals Tup, Tun, Tvp, Tvn, Twp, and Twn are generated by two methods described below.

[0029]

(1) As a switching mode during one carrier period, the conducting time signals Tup, Tun, Tvp, Tvn, Twp, and Twn are generated according to time ratio control for three kinds of vectors in total, namely, two kinds of basic voltage vectors with a phase difference of 120 degrees and a zero vector obtained by switching of only one phase from a switching state of one of the two kinds of basic voltage vectors (this is referred to as "first combination").

[0030]

(2) As a switching mode during one carrier period, the conducting time signals Tup, Tun, Tvp, Tvn, Twp, and Twn are generated according to time ratio control for three kinds of basic voltage vectors having phase differences of 60 degrees, respectively (this is referred to as "second combination"). These methods are explained below with

reference to Figs. 39A to 42.

[0031]

Figs. 39A and 39B are diagrams of a relation between the basic voltage vectors used for a first combination in the PWM-signal creating unit shown in Fig. 36 on a phase plane and an example of an order of switching the basic voltage vectors, respectively. Fig. 40 is a timing chart of an example of a logical state (a switching pattern) of a semiconductor switching element on a DC-bus positive-pole side controlled by the first combination.

[0032]

In the case of the first combination, for example, when an area in which the inverter rotation angle θ is 30 to 90 degrees is considered limitedly, it is possible to generate the conducting time signals Tup, Tun, Tvp, Tvn, Twp, and Twn by using the basic voltage vectors V1 (0, 0, 1) and V2 (0, 1, 0) with a phase difference of 120 degrees and the zero vector V0 (0, 0, 0) as shown in Fig. 39A and switching the vectors in an order of V0, V2, V0, V1, and V0 as shown in Fig. 39B. A logical state (a switching pattern) of the semiconductor switching elements 5a, 5c, and 5e on a DC bus positive pole side in this case is as shown in Fig. 40. It is seen that a state of output to the motor 7 by the driving signals Wp, Vp, and Up, which are given to the semiconductor switching elements 5a, 5c, and 5e by the PWM-signal generating unit 15, changes in the switching order shown in Fig. 39B.

[0033]

Figs. 41A and 41B are diagrams of a relation between the basic voltage vectors used for a second combination in the PWM-signal creating unit shown in Fig. 36 on a phase plane and an example of an order of switching the basic voltage vectors, respectively. Fig. 42 is a timing chart

of an example of a logical state (a switching pattern) of a
semiconductor switching element on a DC-bus positive-pole
side controlled by the second combination.
[0034]

5   In the case of the second combination, for example,
when an area in which the inverter rotation angle θ is 30
to 90 degrees is considered limitedly, it is possible to
generate the conducting time signals Tup, Tun, Tvp, Tvn,
Twp, and Twn by using the basic voltage vectors V1 (0, 0,
10   1), V3 (0, 1, 1), and V2 (0, 1, 0) having phase differences
of 60 degrees and switching the vectors in an order of V3,
V1, V3, V2, and V3 as shown in Fig. 41B. A logical state
(a switching pattern) of the semiconductor switching
elements 5a, 5c, and 5e on a DC bus positive pole side in
15   this case is as shown in Fig. 42. It is seen that a state
of output to the motor 7 by driving the signals Wp, Vp, and
Up, which are given to the semiconductor switching elements
5a, 5c, and 5e by the PWM-signal generating unit 15,
changes in the switching order shown in Fig. 41B.
20   [0035]

Note that, for example, a patent document 2 discloses
a three-phase PWM voltage generating circuit that obtains a
sufficient pulse width by contriving pulse width modulation
when it is difficult to detect a DC bus voltage. A patent
25   document 3 discloses an inverter or the like that makes it
possible to detect an electric current by inserting a
carrier wave for one period when it is necessary to detect
a DC bus voltage. A patent document 4 discloses a PWM
inverter or the like that makes it possible to detect an
30   electric current by preparing a conversion table in advance
and setting a pulse width of a DC bus current to a
predetermined value or more. A patent document 5 discloses
an inverter or the like that makes it possible to perform

sampling of a DC bus current even in an inexpensive
microcomputer by contriving detection timing of the DC bus
current.

[0036]

5 Patent Document 1: Japanese Patent Application Laid-
open No. 7-298631

 Patent Document 2: Japanese Patent No. 3447366

 Patent Document 3: Japanese Patent Application Laid-
open No. 2003-224982

10 Patent Document 4: Japanese Patent Application Laid-
open No. 2003-209976

 Patent Document 5: Japanese Patent Application Laid-
open No. 2002-95263

15 DISCLOSURE OF INVENTION

PROBLEM TO BE SOLVED BY THE INVENTION

[0037]

 However, the conventional extended PWM system has
problems described below. In the system for generating a
20 three-phase PWM signal using three kinds of basic voltage
vectors in total, namely, two kinds of basic voltage
vectors with a phase difference of 120 degrees and a zero
vector not having a magnitude that is obtained by switching
only one phase of switching states of the basic voltage
25 vectors, there is a limitation on a magnitude of a
conducting time signal to be generated. In other words,
there is a limitation on a magnitude of a voltage command
vector used for the next control that can be produced. The
voltage command vector can only be applied to a range with
30 a low percentage modulation. Thus, there is a significant
limitation of use of the system.

[0038]

 In this system, since basic voltage vectors with a

phase difference of 60 degrees is not used, inverter efficiency is deteriorated as a result of feeding an effective current more than necessary. There is a tendency that higher harmonics increases in a motor current and noise and vibration increase. In addition, in this system, there is also a problem in that, when a holding time width of a zero vector is narrowed, an area close to two-phase simultaneous switching is generated to make switching itself unstable.

[0039]

On the other hand, in the system for generating a three-phase PWM signal using three kinds of basic voltage vectors having phase differences of 60 degrees, respectively, since a zero vector is not used, efficiency is deteriorated significantly. In this system, when a width of one basic voltage vector is narrowed, an area close to two-phase simultaneous switching is generated to make switching itself unstable. Thus, a limitation on a range of use of the system is large. In addition, in this system, practically, since there are many limitations of a percentage modulation or a spatial vector rotation angle, there is a problem in that burdens on software increase and, as a result, hardware with high performance is required.

[0040]

The present invention has been devised in view of the circumstances described above and it is an object of the present invention to obtain a three-phase PWM-signal generating apparatus that can increase a holding time width of a switching mode with a simple method having a less limitation of an output voltage range and can reduce a current detection limited range of a DC bus without adding a new device in a three-phase voltage inverter.

MEANS FOR SOLVING PROBLEM

[0041]

An apparatus for generating a three-phase pulse-width-modulation signal for a three-phase voltage inverter employing a semiconductor switching element, according to one aspect of the present invention, includes a generating unit that generates the three-phase pulse-width-modulation signal based on a combination of three basic voltage vectors and a zero vector.

[0042]

According to the present invention, it is possible to generate a PWM signal having a high degree of freedom of a percentage modulation and preventing excessive deterioration of efficiency with a simple method of using three kinds of basic voltage vectors and at least one kind of a zero vector without adding a special device.

EFFECT OF THE INVENTION

[0043]

According to the present invention, there is an effect that it is possible to increase a holding time width of a switching mode with a simple method with a less limitation of an output voltage range without adding a new device and it is possible to generate a three-phase PWM signal in a form of reducing a current detection limited range of a DC bus.

BRIEF DESCRIPTION OF DRAWINGS

[0044]

Fig. 1 is a block diagram of an inverter including a three-phase PWM-signal generating apparatus according to a first embodiment of the present invention;

Figs. 2A to 2C are graphs for explaining an operation

for generating a PWM signal using three basic voltage vectors and one kind of zero vector in a PWM-signal generating unit shown in Fig. 1;

Figs. 3A and 3B are diagrams of a relation between the basic voltage vectors and the zero vector on a phase plane when an inverter rotation angle is near 60 degrees in generating a PWM signal and an example of an order of switching the basic voltage vectors and the zero vector, respectively;

Fig. 4 is a timing chart of an example of a logical state (a switching pattern) of a semiconductor switching element on a DC-bus positive-pole side controlled by switching of the basic voltage vectors and the zero vector shown in Fig. 3B (pattern #1);

Figs. 5A and 5B are diagrams of a relation between the basic voltage vectors and the zero vector on a phase plane when the inverter rotation angle is near 120 degrees in generating a PWM signal and an example of an order of switching the basic voltage vectors and the zero vector, respectively;

Fig. 6 is a timing chart of an example of a logical state (a switching pattern) of a semiconductor switching element on a DC-bus positive-pole side controlled by switching of the basic voltage vectors and the zero vector shown in Fig. 5B (pattern #2);

Figs. 7A and 7B are diagrams of a relation between the basic voltage vectors and the zero vector on a phase plane when the inverter rotation angle is near 180 degrees in generating a PWM signal and an example of an order of switching the basic voltage vectors and the zero vector, respectively;

Fig. 8 is a timing chart of an example of a logical state (a switching pattern) of a semiconductor switching

element on a DC-bus positive-pole side controlled by
switching of the basic voltage vectors and the zero vector
shown in Fig. 7B (pattern #3);

Figs. 9A and 9B are diagrams of a relation between the
basic voltage vectors and the zero vector on a phase plane
when the inverter rotation angle is near 240 degrees in
generating a PWM signal and an example of an order of
switching the basic voltage vectors and the zero vector,
respectively;

Fig. 10 is a timing chart of an example of a logical
state (a switching pattern) of a semiconductor switching
element on a DC-bus positive-pole side controlled by
switching of the basic voltage vectors and the zero vector
shown in Fig. 9B (pattern #4);

Figs. 11A and 11B are diagrams of a relation between
the basic voltage vectors and the zero vector on a phase
plane when the inverter rotation angle is near 300 degrees
in generating a PWM signal and an example of an order of
switching the basic voltage vectors and the zero vector,
respectively;

Fig. 12 is a timing chart of an example of a logical
state (a switching pattern) of a semiconductor switching
element on a DC-bus positive-pole side controlled by
switching of the basic voltage vectors and the zero vector
shown in Fig. 11B (pattern #5);

Figs. 13A and 13B are diagrams of a relation between
the basic voltage vectors and the zero vector on a phase
plane when the inverter rotation angle is near 0 degrees in
generating a PWM signal and an example of an order of
switching the basic voltage vectors and the zero vector,
respectively;

Fig. 14 is a timing chart of an example of a logical
state (a switching pattern) of a semiconductor switching

element on a DC-bus positive-pole side controlled by switching of the basic voltage vectors and the zero vector shown in Fig. 13B (pattern #6);

Fig. 15A is a table of relations between the inverter rotation angle θ and the patterns #1 to #6;

Fig. 15B is a diagram of the relation between the inverter rotation angle θ and the patterns #1 to #6 shown in Fig. 15A on a phase plane;

Figs. 16A and 16B are diagrams of a relation between three basic voltage vectors and two zero vectors on a phase plane when the inverter rotation angle is near 60 degrees in generating a PWM signal using the basic voltage vectors and the zero vectors according to a second embodiment of the present invention and an example of an order of switching the basic voltage vectors and the zero vectors, respectively;

Figs. 17A to 17D are timing charts of logical states (switching patterns) of a semiconductor switching element on a DC-bus positive-pole side controlled by four ways of switching the basic voltage vectors and the zero vectors shown in Fig. 16B (pattern #21);

Figs. 18A and 18B are diagrams of a relation between three basic voltage vectors and two zero vectors on a phase plane when the inverter rotation angle is near 120 degrees in generating a PWM signal using the basic voltage vectors and the zero vectors according to a second embodiment of the present invention and an example of an order of switching the basic voltage vectors and the zero vectors, respectively;

Figs. 19A to 19D are timing charts of logical states (switching patterns) of a semiconductor switching element on a DC-bus positive-pole side controlled by four ways of switching the basic voltage vectors and the zero vectors

shown in Fig. 18B (pattern #22);

Figs. 20A and 20B are diagrams of a relation between three basic voltage vectors and two zero vectors on a phase plane when the inverter rotation angle is near 180 degrees in generating a PWM signal using the basic voltage vectors and the zero vectors according to a second embodiment of the present invention and an example of an order of switching the basic voltage vectors and the zero vectors, respectively;

Figs. 21A to 21D are timing charts of logical states (switching patterns) of a semiconductor switching element on a DC-bus positive-pole side controlled by four ways of switching the basic voltage vectors and the zero vectors shown in Fig. 20B (pattern #23);

Figs. 22A and 22B are diagrams of a relation between three basic voltage vectors and two zero vectors on a phase plane when the inverter rotation angle is near 240 degrees in generating a PWM signal using the basic voltage vectors and the zero vectors according to a second embodiment of the present invention and an example of an order of switching the basic voltage vectors and the zero vectors, respectively;

Figs. 23A to 23D are timing charts of logical states (switching patterns) of a semiconductor switching element on a DC-bus positive-pole side controlled by four ways of switching the basic voltage vectors and the zero vectors shown in Fig. 22B (pattern #24);

Figs. 24A and 24B are diagrams of a relation between three basic voltage vectors and two zero vectors on a phase plane when the inverter rotation angle is near 300 degrees in generating a PWM signal using the basic voltage vectors and the zero vectors according to a second embodiment of the present invention and an example of an order of

switching the basic voltage vectors and the zero vectors, respectively;

Figs. 25A to 25D are timing charts of logical states (switching patterns) of a semiconductor switching element on a DC-bus positive-pole side controlled by four ways of switching the basic voltage vectors and the zero vectors shown in Fig. 24B (pattern #25);

Figs. 26A and 26B are diagrams of a relation between three basic voltage vectors and two zero vectors on a phase plane when the inverter rotation angle is near 0 degrees in generating a PWM signal using the basic voltage vectors and the zero vectors according to a second embodiment of the present invention and an example of an order of switching the basic voltage vectors and the zero vectors, respectively;

Figs. 27A to 27D are timing charts of logical states (switching patterns) of a semiconductor switching element on a DC-bus positive-pole side controlled by four ways of switching the basic voltage vectors and the zero vectors shown in Fig. 26B (pattern #26);

Figs. 28A to 28C are graphs for explaining an operation of a PWM-signal creating unit in a three-phase PWM-signal generating apparatus according to a third embodiment of the present invention;

Fig. 29A is a graph of occurrence time ratios of two basic voltage vectors and a zero vector in a conventional three-phase modulation system or a two-phase modulation system;

Fig. 29B is a graph of occurrence time ratios of three basic voltage vectors and a zero vector according to the third embodiment;

Figs. 30A to 30C are graphs for explaining an operation of a PWM-signal creating unit in a three-phase

PWM-signal generating apparatus according to a fourth
embodiment of the present invention;

Figs. 31A and 31B are diagrams of a relation between
three basic voltage vectors having a phase difference of
5   120 degrees and a zero vector on a phase plane when the
inverter rotation angle is near 60 degrees in generating a
PWM signal according to the fourth embodiment and an
example of an order of switching the basic voltage vectors
and the zero vector, respectively;

10   Figs. 32A and 32B are timing charts of a logical state
(a switching pattern) of a semiconductor switching element
on a DC-bus positive-pole side controlled by two ways of
switching the basic voltage vectors and the zero vector
shown in Fig. 31B (pattern #31);

15   Figs. 33A and 33B are diagrams of a relation between
three basic voltage vectors having a phase difference of
120 degrees and a zero vector on a phase plane when the
inverter rotation angle is near 120 degrees in generating a
PWM signal according to the fourth embodiment and an
20   example of an order of switching the basic voltage vectors
and the zero vector, respectively;

Figs. 34A and 34B are timing charts of a logical state
(a switching pattern) of a semiconductor switching element
on a DC-bus positive-pole side controlled by two ways of
25   switching the basic voltage vectors and the zero vector
shown in Fig. 32B (pattern #32);

Figs. 35A to 35C are graphs for explaining a method of
constituting a PWM-signal generating unit according to a
fifth embodiment of the present invention, when both the
30   methods of generating a PWM signal according to the first
to the fourth embodiments and the method of generating a
PWM signal according to the conventional three-phase
modulation system or two-phase modulation system are used;

Fig. 36 is a block diagram of an example of a conventional inverter;

Fig. 37 is a table of a relation between eight kinds of basic voltage vectors, switching modes corresponding to the basic voltage vectors, and phase currents that can be observed as a DC bus current Idc;

Fig. 38 is a diagram for explaining a phase relation between the basic voltage vectors and a relation between the inverter rotation angle and a voltage command vector;

Figs. 39A and 39B are diagrams of a relation between the basic voltage vectors used for a first combination in the PWM-signal creating unit shown in Fig. 36 on a phase plane and an example of an order of switching the basic voltage vectors, respectively;

Fig. 40 is a timing chart of an example of a logical state (a switching pattern) of a semiconductor switching element on a DC-bus positive-pole side controlled by the first combination;

Figs. 41A and 41B are diagrams of a relation between the basic voltage vectors used for a second combination in the PWM-signal creating unit shown in Fig. 36 on a phase plane and an example of an order of switching the basic voltage vectors, respectively; and

Fig. 42 is a timing chart of an example of a logical state (a switching pattern) of a semiconductor switching element on a DC-bus positive-pole side controlled by the second combination.

EXPLANATIONS OF LETTERS OR NUMERALS

[0045]

1   Inverter main circuit

3   DC power supply

4a, 4b   DC buses

5a, 5b, 5c, 5d, 5e, 5f   semiconductor switching elements

6a, 6b, 6c, 6d, 6e, 6f   Flywheel diodes

7   Motor

9   DC current detecting unit

11   Phase current discriminating unit

12   Unit for calculating an excitation current and a torque current

13   Voltage-command-vector calculating unit

15   PWM-signal generating unit

20   Inverter control unit

21   PWM-signal generating unit

22   PWM-signal-duty creating unit ·

23   PWM-signal-duty redistributing unit

25, 26, 27   Virtual voltage vectors

31, 32, 33   Virtual voltage vectors

35C6, 37 Virtual voltage vectors

41, 42   Switching points

BEST MODE(S) FOR CARRYING OUT THE INVENTION

[0046]

Exemplary embodiments of a three-phase PWM-signal generating apparatus according to the present invention are explained in detail below with reference to the drawings.

[0047]

First embodiment

Fig. 1 is a block diagram of an inverter including a three-phase PWM-signal generating apparatus according to a first embodiment of the present invention. Note that, in Fig. 1, components identical with or equivalent to the components shown in Fig. 36 (the conventional example) are denoted by the identical reference numerals and signs. Sections related to the first embodiment are mainly

explained here.

[0048]

As shown in Fig. 1, in the first embodiment, an inverter control unit 20 is provided instead of the inverter control unit 2 in the constitution shown in Fig. 36 (the conventional example). In the inverter control unit 20, a PWM-signal creating unit 21 is provided instead of the PWM-signal creating unit 14 shown in Fig. 36 (the conventional example).

[0049]

The PWM-signal creating unit 21 includes a PWM-signal-duty creating unit 22, which receives a voltage command vector V* from the voltage-command-vector calculating unit 13, and a PWM-signal-duty redistributing unit 23, which receives an output of the PWM-signal-duty creating unit 22 and outputs conducting time signals Tup, Tun, Tvp, Tvn, Twp, and Twn to the PWM-signal generating unit 15.

[0050]

An operation of the PWM-signal creating unit 21 according to the first embodiment is explained here. Figs. 2A to 2C are graphs for explaining an operation of the PWM-signal creating unit 21. Fig. 2A is a diagram for explaining an operation of the PWM-signal-duty creating unit 22. Fig. 2B is a diagram for explaining a virtual voltage vector used in the PWM-signal-duty redistributing unit 23. Fig. 2C is a diagram for explaining an operation of the PWM-signal-duty redistributing unit 23.

[0051]

The PWM-signal-duty creating unit 22 decomposes the voltage command vector V* from the voltage-command-vector calculating unit 13 in directions of two basic voltage vectors on both sides of the voltage command vector V* to thereby generate production time ratios of the respective

basic voltage vectors. In other words, the PWM-signal-duty
creating unit 22 produces two kinds of basic voltage
vectors with a phase difference of 60 degrees having the
production time ratios as vector lengths and at least one
kind of a zero vector. This system is the same as the
conventional three-phase modulation system or two-phase
modulation system. This is explained specifically with
reference to Fig. 2A.
[0052]

In Fig. 2A, basic voltage vectors V3 and V2 are
arranged at an interval of 60 degrees clockwise on a phase
plane having a direction of the basic voltage vector V1 as
an initial phase. When an inverter rotation angle θ is
near 60 degrees, that is, when the voltage command vector
V* is present between the basic voltage vector V1 and the
basic voltage vector V3 (in Fig. 2A, the voltage command
vector V* is near the basic voltage vector V3). A state of
generation of production time ratios in this case is shown
in Fig. 2A. As shown in Fig. 2A, when the voltage command
vector V* is present between the basic voltage vector V1
and the basic voltage vector V3, the PWM-signal-duty
creating unit 22 decomposes the voltage command vector V*
in two directions of the basic voltage vector V1 and the
basic voltage vector V3 to thereby generate a production
time ratio d1 of the basic voltage vector V1 and a
production time ratio d3 of the basic voltage vector V3.
Although not shown in the figure, a zero vector
corresponding to the voltage command vector V* is also
produced simultaneously.
[0053]

As shown in Fig. 2A, when the voltage command vector
V* is near the basic voltage vector V3, the production time
ratio d3 of the basic voltage vector V3 is long but the

production time ratio d1 of the basic voltage vector V1 is short. Therefore, in the conventional three-phase modulation system or two-phase modulation system, there is a problem in that it is difficult to detect an electric
5   current at the time when the basic voltage vector V1 is produced.

[0054]

Concerning this problem, for example, if PWM signal generation is performed with a combination of the basic
10   voltage vectors V1, V2, and V3 and the zero vector V0 during one carrier control period, it is possible to perform current detection easily even if a percentage modulation is low and apply the current detection to a range in which the percentage modulation is equal to or
15   higher than 0.5. In addition, it is possible to prevent excessive deterioration of efficiency.

[0055]

In other words, if it is possible to generate a PWM signal using three kinds of basic voltage vectors having
20   phase differences of 60 degrees and one kind of a zero vector, the voltage-command-vector calculating unit 13 can produce the voltage command vector V* with a high degree of freedom that makes it easy to detect an electric current and has a less limitation of a percentage modulation and
25   less deterioration of efficiency.

[0056]

However, for a voltage command vector produced by a PWM signal according to such a simple combination of three kinds of basic voltage vectors having phase differences of
30   60 degrees and one kind of a zero vector, it is difficult to set rules for vector production by the simple decomposition in two directions shown in Fig. 2A. Thus, PWM signal generation cannot be performed simply. In this

case, a new rule for decomposing a voltage command vector
in three directions is required.
[0057]

Thus, in the first embodiment, after the vector
production by the decomposition in two directions shown in
Fig. 2A, the voltage command vector is further decomposed
into three basic voltage vectors having phase differences
of 60 degrees and one zero vector using a zero vector such
that rules can be set for vector production. The PWM
signal duty redistribution unit 23 performs this operation.
This is explained below specifically.
[0058]

The zero vector is a vector that does not originally
have a length. It can be considered that the zero vector
may be virtually replaced with a sum of three voltage
vectors with phase differences of 120 degrees having equal
production time ratios as long as a production time allows.
Three voltage vectors having phase differences of 120
degrees with the same vector lengths are hereinafter
referred to as virtual voltage vectors. In Fig. 2B, three
virtual voltage vectors 25, 26, and 27 with phase
differences of 120 degrees having equal production time
ratios d' are superimposed on three basic voltage vectors
V1, V3, and V2 having phase differences of 60 degrees shown
in Fig. 2A. As shown in Fig. 2B, the virtual voltage
vector 25 is in-phase with the basic voltage vector V1, the
virtual voltage vector 26 is anti-phase with the basic
voltage vector V3, and the virtual voltage vector 27 is in-
phase with the basis voltage vector V2.
[0059]

The PWM-signal-duty redistributing unit 23
superimposes three virtual voltage vectors in directions of
basic voltage vectors having phase differences of 120

degrees, respectively, to add up production time ratios of both the virtual voltage vectors and the basic voltage vectors such that a direction of a basic voltage vector, which has a short production time ratio and with which

5   current detection is difficult, of the two kinds of basic voltage vectors produced by the conventional two-phase modulation system or three-phase modulation system shown in Fig. 2Ais included. In the example shown in Fig. 2A, since the production time ratio d1 of the basic voltage vector V1

10   is short, as shown in Fig. 2C, the PWM-signal-duty redistributing unit 23 superimposes the three virtual voltage vectors with the equal production time ratios d' on the basic voltage vector V1, the basic voltage vector V2, and the basic voltage vector V4 (-V3) to add up production

15   time ratios thereof.
     [0060]

         As a result, production time ratios d1', d2', and d3' in the directions of the basic voltage vectors V1, V2, and V3 are as follows: d1'=d1+d', d2'=d', and d3'=d3-d'. A

20   result of the addition does not exceed a value 1. In other words, d1'+d2'+d3'≤1 is a constraint in the PWM-signal-duty redistributing unit 23. According to such simple processing, it is possible to increase the production time ratio of the basic voltage vector V1, which is short in the

25   conventional system shown in Fig. 2A, by a magnitude of the virtual voltage vector. This makes it easy to perform current detection. The PWM-signal-duty redistributing unit 23 redistributes a production time ratio of a voltage command vector to three kinds of basic voltage vectors

30   having phase differences of 60 degrees and one zero vector using a zero vector under a condition that a result of addition is equal to or smaller than the value 1.
     [0061]

A three-phase PWM signal produced by the simple method described above is specifically explained with reference to Figs. 3A to 14. Figs. 3A and 3B are diagrams of a relation on a phase plane at the time when an inverter rotation

5　angle is near 60 degrees in generating a PWM signal using three kinds of basic voltage vectors and one kind of a zero vector and an example of an order of switching of the three kinds of basic voltage vectors and the one kind of a zero vector. Fig. 4 is a timing chart of an example of a

10　logical state (a switching pattern) of semiconductor switching elements on a DC bus positive pole side controlled according to the switching of the three kinds of basic voltage vectors and the one kind of a zero vector shown in Fig. 3B.

15　[0062]

In Fig. 3A, the basic voltage vector V3 (0, 1, 1), the basic voltage vector V2 (0, 1, 0), and the zero vector V0 (0, 0, 0), which relate to one another when the inverter rotation angle θ is near 60 degrees with the basic voltage

20　vector V1 (0, 0, 1) as an initial phase, are shown. When the inverter rotation angle θ is near 60 degrees, as shown in Fig. 3B, it is possible to generate the conducting time signals Tup, Tun, Tvp, Tvn, Twp, and Twn by switching the basic voltage vectors and the zero vector in an order of V0,

25　V1, V3, V2, V0, and V1. Note that, opposite to Fig. 3B, the basic voltage vectors and the zero vector may be .switched in an order of V0, V2, V3, V1, V0, and V2.
[0063]

A logical state (a switching pattern) during one

30　carrier control period of semiconductor switching elements 5a, 5c, and 5e on a DC bus positive pole side at the time when the basic voltage vectors and the zero vector are switched as shown in Fig. 3B are as shown in Fig. 4. This

is set as a pattern #1. It is seen that a state of output to the motor 7 by driving signals Wp, Vp, and Up given to the semiconductor switching elements 5a, 5c, and 5e by the PWM-signal generating unit 15 changes in the switching

5   order shown in Fig. 3B.

[0064]

When the example of Fig. 2C is applied to Fig. 4, a conducting time ratio of a U-phase positive pole side switching element is d1'+d3'. A conducting time ratio of a

10 V-phase positive pole side switching element is d2'+d3'. A conducting time ratio of a W-phase positive pole side switching element is 0. In other words, the W-phase positive pole side switching element is always in an OFF operation state. Conducting time ratios of negative pole

15 side switching elements 5b, 5d, and 5f in the respective phases are calculated by subtracting the conducting time ratios of the positive pole side switching elements 5a, 5c, and 5e from the value 1. Conducting times during one carrier control period of the respective switching elements

20 are decided by multiplying these values by one carrier control period.

[0065]

In this way, the PWM-signal-duty redistributing unit 23 obtains the conducting times Tup, Tvp, and Twp during

25 one carrier control period of the U-phase, V-phase, and W-phase positive pole side switching elements 5a, 5c, and 5e and the conducting times Tun, Tvn, and Twn during one carrier control period of the negative pole side switching elements 5b, 5d and 5f. Based on the conducting times, the

30 PWM-signal generating unit 15 emits driving signals Up, Vp, Wp, Un, Vn, and Wn to the semiconductor switching elements 5a, 5c, 5e, 5b, 5d, and 5f to make it possible to drive the motor 7.

[0066]

Similarly, it is also possible to show a generation state of a PWM signal, with the basic voltage vector V1 as an initial phase, at the time when the inverter rotation angle θ is near 120 degrees (in a direction of the basic voltage vector V2) (Figs. 5A to 6), at the time when the inverter rotation angle θ is near 180 degrees (in a direction of the basic voltage vector V6) (Figs. 7A to 8), at the time when the inverter rotation angle θ is near 240 degrees (in a direction of the basic voltage vector V4) (Figs. 9A to 10), at the time when the inverter rotation angle θ is near 300 degrees (in a direction of the basic voltage vector V5) (Figs. 11A to 12), and at the time when the inverter rotation angle θ is near 0 degree (in a direction of the basic voltage vector V1) (Figs. 13A to 14).

[0067]

Figs. 5A and 5B are diagrams of a relation on a phase plane at the time when the inverter rotation angle θ is near 120 degrees in generating a PWM signal using three kinds of basic voltage vectors and one kind of a zero vector and an example of an order of switching of the three kinds of basic voltage vectors. Fig. 6 is a timing chart of an example of a logical state (a switching pattern) of semiconductor switching elements on a DC bus positive pole side controlled according to the switching of the three kinds of basic voltage vectors shown in Fig. 5B.

[0068]

In Fig. 5A, the basic voltage vector V3 (0, 1, 1), the basic voltage vector V2 (0, 1, 0), the basic voltage vector V6 (1, 1, 0), and the zero vector V7 (1, 1, 1), which relate to one another when the inverter rotation angle θ is near 120 degrees, are shown. When the inverter rotation

angle θ is near 120 degrees, as shown in Fig. 5B, it is
possible to generate the conducting time signals Tup, Tun,
Tvp, Tvn, Twp, and Twn by switching the basic voltage
vectors and the zero vector in an order of V7, V3, V2, V6,
V7, and V3. Note that, opposite to Fig. 5B, the basic
voltage vectors and the zero vector may be switched in an
order of V7, V6, V2, V3, V7, and V6.
[0069]

A logical state (a switching pattern) during one
carrier control period of the semiconductor switching
elements 5a, 5c, and 5e on a DC bus positive pole side at
the time when the basic voltage vectors and the zero vector
are switched as shown in Fig. 5B are as shown in Fig. 6.
This is set as a pattern #2. It is seen that a state of
output to the motor 7 by the driving signals Wp, Vp, and Up
given to the semiconductor switching elements 5a, 5c, and
5e by the PWM-signal generating unit 15 changes in the
switching order shown in Fig. 5B. In this case, the V-
phase positive pole side semiconductor switching element is
always in an ON operation state.
[0070]

Figs. 7A and 7B are diagrams of a relation on a phase
plane at the time when the inverter rotation angle θ is
near 180 degrees in generating a PWM signal using three
kinds of basic voltage vectors and one kind of a zero
vector and an example of an order of switching of the three
kinds of basic voltage vectors. Fig. 8 is a timing chart
of an example of a logical state (a switching pattern) of
semiconductor switching elements on a DC bus positive pole
side controlled according to the switching of the three
kinds of basic voltage vectors shown in Fig. 7B.
[0071]

In Fig. 7A, the basic voltage vector V2 (0, 1, 0), the

basic voltage vector V6 (1, 1, 0), the basic voltage vector
V4 (1, 0, 0), and the zero vector V0 (0, 0, 0), which
relate to one another when the inverter rotation angle θ is
near 180 degrees, are shown. When the inverter rotation
angle θ is near 180 degrees, as shown in Fig. 7B, it is
possible to generate the conducting time signals Tup, Tun,
Tvp, Tvn, Twp, and Twn by switching the basic voltage
vectors and the zero vector in an order of V0, V2, V6, V4,
V0, and V2. Note that, opposite to Fig. 7B, the basic
voltage vectors and the zero vector may be switched in an
order of V0, V4, V6, V2, V0, and V4.
[0072]

A logical state (a switching pattern) during one
carrier control period of the semiconductor switching
elements 5a, 5c, and 5e on a DC bus positive pole side at
the time when the basic voltage vectors and the zero vector
are switched as shown in Fig. 7B are as shown in Fig. 8.
This is set as a pattern #3. It is seen that a state of
output to the motor 7 by the driving signals Wp, Vp, and Up
given to the semiconductor switching elements 5a, 5c, and
5e by the PWM-signal generating unit 15 changes in the
switching order shown in Fig. 7B. In this case, the U-
phase positive pole side semiconductor switching element is
always in an OFF operation state.
[0073]

Figs. 9A and 9B are diagrams of a relation on a phase
plane at the time when the inverter rotation angle θ is
near 240 degrees in generating a PWM signal using three
kinds of basic voltage vectors and one kind of a zero
vector and an example of an order of switching of the three
kinds of basic voltage vectors. Fig. 10 is a timing chart
of an example of a logical state (a switching pattern) of

semiconductor switching elements on a DC bus positive pole side controlled according to the switching of the three kinds of basic voltage vectors shown in Fig. 9B.

[0074]

In Fig. 9A, the basic voltage vector V6 (1, 1, 0), the basic voltage vector V4 (1, 0, 0), the basic voltage vector V5 (1, 0, 1), and the zero vector V7 (1, 1, 1), which relate to one another when the inverter rotation angle θ is near 240 degrees, are shown. When the inverter rotation angle θ is near 240 degrees, as shown in Fig. 9B, it is possible to generate the conducting time signals Tup, Tun, Tvp, Tvn, Twp, and Twn by switching the basic voltage vectors and the zero vector in an order of V7, V6, V4, V5, V7, and V6. Note that, opposite to Fig. 9B, the basic voltage vectors and the zero vector may be switched in an order of V7, V5, V4, V6, V7, and V5.

[0075]

A logical state (a switching pattern) during one carrier control period of the semiconductor switching elements 5a, 5c, and 5e on a DC bus positive pole side at the time when the basic voltage vectors and the zero vector are switched as shown in Fig. 9B are as shown in Fig. 10. This is set as a pattern #4. It is seen that a state of output to the motor 7 by the driving signals Wp, Vp, and Up given to the semiconductor switching elements 5a, 5c, and 5e by the PWM-signal generating unit 15 changes in the switching order shown in Fig. 9B. In this case, the W-phase positive pole side semiconductor switching element is always in an ON operation state.

[0076]

Figs. 11A and 11B are diagrams of a relation on a phase plane at the time when the inverter rotation angle θ

is near 300 degrees in generating a PWM signal using three
kinds of basic voltage vectors and one kind of a zero
vector and an example of an order of switching of the three
kinds of basic voltage vectors. Fig. 12 is a timing chart

5   of an example of a logical state (a switching pattern) of
semiconductor switching elements on a DC bus positive pole
side controlled according to the switching of the three
kinds of basic voltage vectors shown in Fig. 11B.
[0077]

10   In Fig. 11A, the basic voltage vector V4 (1, 0, 0),
the basic voltage vector V5 (1, 0, 1), the basic voltage
vector V1 (0, 0, 1), and the zero vector V0 (0, 0, 0),
which relate to one another when the inverter rotation
angle θ is near 300 degrees, are shown. When the inverter

15 rotation angle θ is near 300 degrees, as shown in Fig. 11B,
it is possible to generate the conducting time signals Tup,
Tun, Tvp, Tvn, Twp, and Twn by switching the basic voltage
vectors and the zero vector in an order of V0, V4, V5, V1,
V0, and V4. Note that, opposite to Fig. 11B, the basic

20 voltage vectors and the zero vector may be switched in an
order of V0, V1, V5, V4, V0, and V1.
[0078]

    A logical state (a switching pattern) during one
carrier control period of the semiconductor switching

25 elements 5a, 5c, and 5e on a DC bus positive pole side at
the time when the basic voltage vectors and the zero vector
are switched as shown in Fig. 11B are as shown in Fig. 12.
This is set as a pattern #5. It is seen that a state of
output to the motor 7 by the driving signals Wp, Vp, and Up

30 given to the semiconductor switching elements 5a, 5c, and
5e by the PWM-signal generating unit 15 changes in the
switching order shown in Fig. 11B. In this case, the V-
phase positive pole side semiconductor switching element is

always in an OFF operation state.

[0079]

Figs. 13A and 13B are diagrams of a relation on a phase plane at the time when the inverter rotation angle θ is near 0 degree in generating a PWM signal using three kinds of basic voltage vectors and one kind of a zero vector and an example of an order of switching of the three kinds of basic voltage vectors. Fig. 14 is a timing chart of an example of a logical state (a switching pattern) of semiconductor switching elements on a DC bus positive pole side controlled according to the switching of the three kinds of basic voltage vectors shown in Fig. 13B.

[0080]

In Fig. 13A, the basic voltage vector V5 (1, 0, 1), the basic voltage vector V1 (0, 0, 1), the basic voltage vector V3 (0, 1, 1), and the zero vector V7 (1, 1, 1), which relate to one another when the inverter rotation angle θ is near 0 degree, are shown. When the inverter rotation angle θ is near 0 degree, as shown in Fig. 13B, it is possible to generate the conducting time signals Tup, Tun, Tvp, Tvn, Twp, and Twn by switching the basic voltage vectors and the zero vector in an order of V7, V5, V1, V3, V7, and V5. Note that, opposite to Fig. 13B, the basic voltage vectors and the zero vector may be switched in an order of V7, V3, V1, V5, V7, and V3.

[0081]

A logical state (a switching pattern) during one carrier control period of the semiconductor switching elements 5a, 5c, and 5e on a DC bus positive pole side at the time when the basic voltage vectors and the zero vector are switched as shown in Fig. 13B are as shown in Fig. 14. This is set as a pattern #6. It is seen that a state of

output to the motor 7 by the driving signals Wp, Vp, and Up given to the semiconductor switching elements 5a, 5c, and 5e by the PWM-signal generating unit 15 changes in the switching order shown in Fig. 13B. In this case, the U-phase positive pole side semiconductor switching element is always in an ON operation state.

[0082]

The method of generating a PWM signal using three kinds of basic voltage vectors having phase differences of 60 degrees and one kind of a zero vector is particularly effective when the inverter rotation angle θ is near integer times of 60 degrees, that is, near the basic voltage vectors V1 to V6. Thus, it is advisable to perform switching of the patterns #1 to #6 near the middle of two basic voltage vectors having a phase difference of 60 degrees. This is represented as a general Equation as follows.

[0083]

When the inverter rotation angle θ located in the middle of two basic voltage vectors having a phase difference of 60 degrees is assumed to be at a switching phase angle $\theta\alpha$ with respect to the inverter rotation angle θ with the direction of the basic voltage vector V1 as an initial phase, the switching phase angle $\theta\alpha$ can be represented as $\theta\alpha=30+60\times n$ using an integer n.

[0084]

Fig. 15A is a table of a relation between the inverter rotation angle θ and the patterns #1 to #6. Fig. 15B is a diagram of the relation between the inverter rotation angle θ and the patterns #1 to #6 on a phase plane. As shown in Figs. 15A and 15B, the inverter rotation angle θ with the direction of the basic voltage vector V1 as an initial

phase is the pattern #6 shown in Fig. 14 at 0°≤θ<30°, the pattern #1 shown in Fig. 4 at 30°≤θ<90°, the pattern #2 shown in Fig. 6 at 90°≤θ<150°, the pattern #3 shown in Fig. 8 at 150°≤θ<210°, the pattern #4 shown in Fig. 10 at 210°≤θ<270°, the pattern #5 shown in Fig. 12 at 270°≤θ<330°, and the pattern #6 shown in Fig. 14 at 330°≤θ<360°. Note that, in Fig. 15A, ranges of the respective patterns are represented as "A degrees or more and B degrees or less". However, an end point of a range may be included in either side.

[0085]

In this way, according to the first embodiment, it is possible to generate a PWM signal having a high degree of freedom of a percentage modulation and preventing excessive deterioration of efficiency with the simple method of using three kinds of basic voltage vector having phase differences of 60 degrees and one kind of a zero vector without adding a special device.

[0086]

In the above explanation, a PWM signal is generated with a combination of three kinds of basic voltage vectors having phase differences of 60 degrees and one kind of a zero vector. However, it is possible to generate a PWM signal in the same idea when two kinds of zero vectors are used. This is explained specifically as a second embodiment.

[0087]

Second embodiment

In an inverter including a three-phase PWM-signal generating apparatus according to a second embodiment of the present invention, a PWM-signal generating unit in the three-phase PWM-signal generating apparatus corresponds to

the PWM-signal creating unit 21 in the constitution shown
in Fig. 1 (the first embodiment). First, an operation of
the PWM-signal-duty creating unit 22 is explained briefly
with reference to Figs. 1 and 2A, although the explanation
5 is redundant.
[0088]

As explained in the first embodiment, the PWM-signal-
duty creating unit 22 decomposes the voltage command vector
V* from the voltage-command-vector calculating unit 13 in
10 directions of two basic voltage vectors on both sides of
the voltage command vector V* to thereby generate
production time ratios of the respective basic voltage
vectors. In other words, the PWM-signal-duty creating unit
22 produces two kinds of basic voltage vectors with a phase
15 difference of 60 degrees having the production time ratios
as vector lengths and at least one kind of a zero vector.
[0089]

In the example shown in Fig. 2A, in a phase plane with
the direction of the basic voltage vector V1 as an initial
20 phase, when the inverter rotation angle θ is near 60
degrees, that is, when the voltage command vector V* is
present between the basic voltage vector V1 and the basic
voltage vector V3 (in Fig. 2A, the voltage command vector
V* is near the basic voltage vector V3), the PWM-signal-
25 duty creating unit 22 decomposes the voltage command vector
V* in two directions of the basic voltage vector V1 and the
basic voltage vector V3 to generate a production time ratio
d1 of the basic voltage vector V1, a production time ratio
d3 of the basic voltage vector V3, and a production time
30 ratio dzero of a zero vector corresponding to the voltage
command vector V*, although the production time ratio dzero
cannot be shown in the figure. This production time ratio
dzero of the zero vector is produced in a relation of

dzero=1-d1-d3.

[0090]

As explained in the first embodiment, the conventional three-phase modulation system or two-phase modulation system shown in Fig. 2A has a problem in that it is difficult to detect an electric current at the time when the basic voltage vector V1 is produced. In the first embodiment coping with this problem, there is a state in which only one set of the three-phase semiconductor switching elements (5a, 5b), (5c, 5d), and (5e, 5f) does not perform switching (see Figs. 3, 6, 8, 10, 12, and 14), a switching balance of three phases cannot be kept and there is a problem in vibration and noise.

[0091]

Thus, in this second embodiment, to cope with both the problems, PWM signal generation is performed with, for example, a combination of the basic voltage vectors V1, V2, and V3 and the zero vectors V0 and V7 during one carrier control period. Consequently, the voltage-command-vector calculating unit 13 can produce the voltage command vector V* with a high degree of freedom that makes it easy to detect an electric current, has a less limitation of a percentage modulation and less deterioration of efficiency, and has a vibration/noise reduction effect.

[0092]

When PWM signal generation is performed with such a combination of three kinds of basic voltage vectors and two kinds of zero vectors, it is also possible to use the method of producing vectors according to two-direction decomposition and, then, further performing vector redistribution by a zero vector shown in Fig. 2A. In other words, the PWM-signal-duty redistributing unit 23 according to the second embodiment performs an operation for

redistributing a production time ratio of the voltage command vector V* to three kinds of basic voltage vectors and two kinds of zero vectors in the same idea as explained in the first embodiment. This is explained in detail below
5   using the three kinds of basic voltage vectors V1, V2, and V3 shown in Fig. 2A.

[0093]

When production time ratios of the three kinds of basic voltage vectors V1, V2, and V3 are d1', d2', and d3',
10   a total production time ratio dzero' of the two kinds of zero vectors after redistribution is represented as follows.

$$Dzero'=1-d1'-d2'-d3' \tag{3}$$

A relation among the total production time ratio dzero', a production time ratio d0' of one zero vector V0, and a
15   production time ratio d7' of the other zero vector V7 is represented as follows when k is assumed to be an arbitrary value within a range of 0 to 1.

$$d0'=k \cdot dzero' \tag{4}$$

$$d7'=(1-k) \cdot dzero' \tag{5}$$

20   [0094]

From Equations (4) and (5), concerning the respective production time ratios of the two kinds of zero vectors, it is possible to divide the total production time ratio dzero' at an arbitrary ratio, set one divided production
25   time ratio as the production time ratio d0' of the zero vector V0, and set the other divided production time ratio as the production time ratio d7' of the zero vector V7. In this way, it is also possible to satisfy Equation (3) by allocating the total production time ratio dzero' to the
30   respective production time ratios of the two kinds of zero vectors.

[0095]

Consequently, the state in which only one set of the

three phase semiconductor switching elements (5a, 5b), (5c, 5d), and (5e, 5f) does not perform switching is eliminated (see Figs. 17, 19, 21, 23, 25, and 27). As a result, since a switching balance of three phases is kept, it is possible to reduce vibration and noise. If a ratio of zero vectors to be divided into to is further changed every moment, it is possible to disperse peak sound near a carrier frequency compared with the time when the ratio is not changed. An acoustic noise reduction effect is obtained.

[0096]

A three-phase PWM signal generated by a method according to the second embodiment is explained specifically with reference to Figs. 16A to 27D. Figs. 16A and 16B are diagrams of a relation on a phase plane at the time when an inverter rotation angle is near 60 degrees in generating a PWM signal using three kinds of basic voltage vectors and two kinds of zero vectors according to a second embodiment of the present invention and an example of an order of switching of the three kinds of basic voltage vectors and the two kinds of zero vectors. Figs. 17A to 17D are timing charts of logical states (switching patterns) of semiconductor switching elements on a DC bus positive pole side controlled according to four ways of the switching of the three kinds of basic voltage vectors and the two kinds of zero vectors shown in Fig. 16B.

[0097]

In Fig. 16A, with the basic voltage vector V1 (0, 0, 1) as an initial phase, the basic voltage vector V3 (0, 1, 1), the basic voltage vector V2 (0, 1, 0), the zero vector V0 (0, 0, 0), and the zero vector V7 (1, 1, 1), which relate to one another when the inverter rotation angle θ is near 60 degrees, are shown. It is possible to generate the conducting time signals Tup, Tun, Tvp, Tvn, Twp, and Twn by

adopting, as shown in Fig. 16B, for example, any one of (a) V7, V3, V1, V0, and V2, (b) V7, V3, V1, V0, V2, and V3, (c) V7, V3, V2, V0, and V1, and (d) V7, V3, V2, V0, V1, and V3 as a switching order at the time when the inverter rotation angle θ is near 60 degrees. This is set as a pattern #21.
[0098]

Figs. 17A to 17D are time charts of logical states (switching patterns) during one carrier control period of the semiconductor switching elements 5a, 5c, and 5e on a DC bus positive pole side in the switching orders (a), (b), (c), and (d) shown in Fig. 16B. As shown in Figs. 17A to 17D, it is possible to drive the three-phase semiconductor switching elements (5a, 5b), (5c, 5d), and (5e, 5f) to turn ON and OFF without a state in which one set of the three-phase semiconductor switching elements does not perform switching.
[0099]

Note that the switching orders in (a) to (d) may be reversed. Specifically, in the example of the switching order (a), the switching order may be V2, V0, V1, V3, and V7. Moreover, a switching direction of the switching order may be reversed for each carrier period. In the example of the switching order (a), it is possible that the switching order is V7, V3, V1, V0, and V2 in a certain carrier period and is V2, V0, V1, V3, and V7 in the next carrier control period. The same applies to Figs. 18B, 20 B, 22 B, 24 B, and 26 B described below.
[0100]

When the example of Fig. 2C is applied to Fig. 17A, a conducting time ratio of the U-phase positive pole side switching element is $d1'+d3'+d7'$. A conducting time ratio of the V-phase positive pole side switching element is $d2'+d3'+d7'$. A conducting time ratio of the W-phase

positive pole side switching element is d7'. Conducting time ratios of negative pole side switching elements in the respective phases are calculated by subtracting the conducting time ratios of the positive pole side switching elements from the value 1. Conducting times during one carrier control period of the respective switching elements are decided by multiplying these values by one carrier control period. At the time of actual PWM signal output, a PWM signal is generated taking into account a short circuit prevention time of a switching element.

[0101]

In this way, the PWM-signal-duty redistributing unit 23 shown in Fig. 1 obtains the conducting times Tup, Tvp, and Twp during one carrier control period of the U-phase, V-phase, and W-phase positive pole side switching elements and the conducting times Tun, Tvn, and Twn during one carrier control period of the negative pole side switching elements. Based on the conducting times, the PWM-signal generating unit 15 emits driving signals Up, Vp, Wp, Un, Vn, and Wn to the semiconductor switching elements 5a, 5c, 5e, 5b, 5d, and 5f to make it possible to drive the motor 7.

[0102]

Similarly, it is also possible to show a generation state of a PWM signal, with the basic voltage vector V1 as an initial phase, at the time when the inverter rotation angle θ is near 120 degrees (in a direction of the basic voltage vector V2) (Figs. 18A to 19D), at the time when the inverter rotation angle θ is near 180 degrees (in a direction of the basic voltage vector V6) (Figs. 20A to 21D), at the time when the inverter rotation angle θ is near 240 degrees (in a direction of the basic voltage vector V4) (Figs. 22A to 23D), at the time when the

inverter rotation angle θ is near 300 degrees (in a direction of the basic voltage vector V5) (Figs. 24A to 25D), and at the time when the inverter rotation angle θ is near 0 degree (in a direction of the basic voltage vector

5   V1) (Figs. 26A to 27D). Since generation of a driving signal can be performed in the same ideal as the pattern #21 described above, an explanation of the generation of a driving signal is omitted but an outline thereof is described below.

10   [0103]

In Fig. 18A, the basic voltage vector V3 (0, 1, 1), the basic voltage vector V2 (0, 1, 0), the basic voltage vector V6 (1, 1, 0), the zero vector V0 (0, 0, 0), and the zero vector V7 (1, 1, 1), which relate to one another on a

15   phase plane at the time when the inverter rotation angle θ with the basic voltage vector V1 as an initial phase is near 120 degrees in generating a PWM signal using three kinds of basic voltage vectors and two kinds of zero vectors according to the second embodiment of the present

20   invention, are shown. In Fig. 18B, as examples of a switching order of three kinds of basic voltage vectors and two kinds of zero vectors, four ways of switching orders, (a) V7, V3, V0, V2, and V6, (b) V7, V3, V2, V0, V2, and V6, (c) V7, V6, V0, V2, and V3, and (d) V7, V6, V2, V0, V2, and

25   V3 are shown. In Figs. 19A to 19D, logical states (switching patterns) of semiconductor switching elements on a DC bus positive pole side controlled according to the switching of four ways of three kinds of basic voltage vectors and two kinds of zero vectors shown in Fig. 18B is

30   shown. This is set as a pattern #22.
[0104]

In Fig. 20A, the basic voltage vector V2 (0, 1, 0),

the basic voltage vector V6 (1, 1, 0), the basic voltage
vector V4 (1, 0, 0), the zero vector V0 (0, 0, 0), and the
zero vector V7 (1, 1, 1), which relate to one another on a
phase plane at the time when the inverter rotation angle θ
5 with the basic voltage vector V1 as an initial phase is
near 180 degrees in generating a PWM signal using three
kinds of basic voltage vectors and two kinds of zero
vectors according to the second embodiment of the present
invention, are shown. In Fig. 20B, as examples of a
10 switching order of three kinds of basic voltage vectors and
two kinds of zero vectors, four ways of switching orders,
(a) V7, V6, V2, V0, and V4, (b) V7, V6, V2, V0, V4, and V6,
(c) V7, V6, V4, V0, and V2, and (d) V7, V6, V4, V0, V2, and
V6 are shown. In Figs. 21A to 21D, a logical state (a
15 switching pattern) of semiconductor switching elements on a
DC bus positive pole side controlled according to the
switching of four ways of three kinds of basic voltage
vectors and two kinds of zero vectors shown in Fig. 20B is
shown. This is set as a pattern #23.
20 [0105]

In Fig. 22A, the basic voltage vector V6 (1, 1, 0),
the basic voltage vector V4 (1, 0, 0), the basic voltage
vector V5 (1, 0, 1), the zero vector V0 (0, 0, 0), and the
zero vector V7 (1, 1, 1), which relate to one another on a
25 phase plane at the time when the inverter rotation angle θ
with the basic voltage vector V1 as an initial phase is
near 240 degrees in generating a PWM signal using three
kinds of basic voltage vectors and two kinds of zero
vectors according to the second embodiment of the present
30 invention, are shown. In Fig. 22B, as examples of a
switching order of three kinds of basic voltage vectors and
two kinds of zero vectors, four ways of switching orders,
(a) V7, V6, V0, V4, and V5, (b) V7, V6, V4, V0, V4, and V5,

(c) V7, V5, V0, V4, and V6, and (d) V7, V5, V4, V0, V4, and V6 are shown. In Figs. 23A to 23D, logical states (switching patterns) of semiconductor switching elements on a DC bus positive pole side controlled according to the switching of four ways of three kinds of basic voltage vectors and two kinds of zero vectors shown in Fig. 22B is shown. This is set as a pattern #24.

[0106]

In Fig. 24A, the basic voltage vector V4 (1, 0, 0), the basic voltage vector V5 (1, 0, 1), the basic voltage vector V1 (0, 0, 1), the zero vector V0 (0, 0, 0), and the zero vector V7 (1, 1, 1), which relate to one another on a phase plane at the time when the inverter rotation angle θ with the basic voltage vector V1 as an initial phase is near 300 degrees in generating a PWM signal using three kinds of basic voltage vectors and two kinds of zero vectors according to the second embodiment of the present invention, are shown. In Fig. 24B, as examples of a switching order of three kinds of basic voltage vectors and two kinds of zero vectors, four ways of switching orders, (a) V7, V5, V4, V0, and V1, (b) V7, V5, V4, V0, V1, and V5, (c) V7, V5, V1, V0, and V4, and (d) V7, V5, V1, V0, V4, and V5 are shown. In Figs. 25A to 25D, logical states (switching patterns) of semiconductor switching elements on a DC bus positive pole side controlled according to the switching of four ways of three kinds of basic voltage vectors and two kinds of zero vectors shown in Fig. 24B is shown. This is set as a pattern #25.

[0107]

In Fig. 26A, the basic voltage vector V5 (1, 0, 1), the basic voltage vector V1 (0, 0, 1), the basic voltage vector V3 (0, 1, 1), the zero vector V0 (0, 0, 0), and the zero vector V7 (1, 1, 1), which relate to one another on a

phase plane at the time when the inverter rotation angle θ with the basic voltage vector V1 as an initial phase is near 0 degree in generating a PWM signal using three kinds of basic voltage vectors and two kinds of zero vectors

5   according to the second embodiment of the present invention, are shown. In Fig. 26B, as examples of a switching order of three kinds of basic voltage vectors and two kinds of zero vectors, four ways of switching orders, (a) V7, V5, V0, V1, and V3, (b) V7, V5, V1, V0, V1, and V3, (c) V7, V3, V0,

10   V1, and V5, and (d) V7, V3, V1, V0, V1, and V5 are shown. In Figs. 27A to 27D, logical states (switching patterns) of semiconductor switching elements on a DC bus positive pole side controlled according to the switching of four ways of three kinds of basic voltage vectors and two kinds of zero

15   vectors shown in Fig. 26B is shown. This is set as a pattern #26.

[0108]

       The method of generating a PWM signal using three kinds of basic voltage vectors and two kinds of zero

20   vectors is also particularly effective when the inverter rotation angle θ is near integer times of 60 degrees (near the basic voltage vectors). Thus, it is advisable to perform switching of the respective patterns near the middle of two basic voltage vectors having a phase

25   difference of 60 degrees as in the first embodiment.

[0109]

       As explained in the first embodiment, for example, a switching phase angle θα is defined as θα=30+60×n (n: integer) and an inverter rotation angle range corresponding

30   to the six patterns, the patterns #21 to #26, is determined as shown in Figs. 15A and 15B. Consequently, it is possible to generate a PWM signal having a high degree of

freedom of a percentage modulation, preventing excessive deterioration of efficiency, and having a noise reduction effect using three kinds of basic voltage vector and two kinds of zero vectors.

5 [0110]

When it is desired to improve a degree of freedom of PWM signal generation in addition to such an effect, it is possible to realize this by setting the switching phase angle $\theta\alpha$ as $\theta\alpha=30\times n$ (n: integer) and switching the

10 switching orders (the switching patterns) shown in Figs. 16B, 18B, 20B, 22B, 24B, and 26B for each section of 30 degrees.

[0111]

Specifically, the switching patterns of (c) and (d)

15 shown in Fig. 16B are used in a section of 30 degrees to 60 degrees and the switching patterns of (a) and (b) shown in Fig. 16B are used in a section of 60 degrees to 90 degrees. Similarly, the switching patterns of (a) and (b) shown in Fig. 18B are used in a section of 90 degrees to 120 degrees

20 and the switching patterns of (c) and (d) shown in Fig. 18B are used in a section of 120 degrees to 150 degrees. The switching patterns of (c) and (d) shown in Fig. 20B are used in a section of 150 degrees to 180 degrees and the switching patterns of (a) and (b) shown in Fig. 20B are

25 used in a section of 180 degrees to 210 degrees. The switching patterns of (a) and (b) shown in Fig. 22B are used in a section of 210 degrees to 240 degrees and the switching patterns of (c) and (d) shown in Fig. 22B are used in a section of 240 degrees to 270 degrees. The

30 switching patterns of (c) and (d) shown in Fig. 24B are used in a section of 270 degrees to 300 degrees and the switching patterns of (a) and (b) shown in Fig. 24B are used in a section of 300 degrees to 330 degrees. The

switching patterns of (a) and (b) shown in Fig. 26B are used in a section of 330 degrees and 360 degrees and the switching patterns of (c) and (d) shown in Fig. 26B are used in a section of 0 degree to 30 degrees.

5 [0112]

In this way, according to the second embodiment, as in the first embodiment, it is possible to generate a PWM signal having a high degree of freedom of a percentage modulation and preventing excessive deterioration of

10 efficiency with the simple method of using three kinds of basic voltage vector having phase differences of 60 degrees and two kinds of zero vectors without adding a special device. It is also possible to generate a PWM signal also having a noise reduction effect in addition to the effect

15 in the first embodiment.

[0113]

Note that it is possible to switch and use the PWM signal generating system according to the first embodiment using one kind of a zero vector and the PWM signal

20 generating system according to the second embodiment using two kinds of zero vectors as required. It is possible to realize this by, for example, selecting the systems for each arbitrary section of an inverter rotation angle or changing the systems at arbitrary timing at the time of

25 generation of a PWM signal.

[0114]

Third embodiment

Figs. 28A to 28C are graphs for explaining, in an inverter including a three-phase PWM-signal generating

30 apparatus according to a third embodiment of the present invention, an operation of a PWM-signal generating unit in the three-phase PWM-signal generating apparatus. In the third embodiment, a PWM signal is generated by the same

method as the first and the second embodiment. However, an example of a constitution in securing an operation range on a low speed side of a motor is shown in the third embodiment. To facilitate understanding, in the

5 explanation of the second embodiment, a PWM signal is generated by the method according to the first embodiment.
[0115]

In the third embodiment, in the PWM-signal creating unit 21 in the constitution shown in Fig. 1 (the first

10 embodiment), the PWM-signal-duty creating unit 22 performs the same operation as the first embodiment. However, the PWM-signal-duty redistributing unit 23 performs an operation different from the operation in the first embodiment. The third embodiment is explained below with

15 reference to Fig. 1.
[0116]

To secure an operation range on a low speed side of the motor 7, it is necessary to further reduce a percentage modulation, that is, further reduce a length |V*| of the

20 voltage command vector V*. To make such control possible, it is necessary to secure a production time ratio of a basic voltage vector for performing current detection. Originally, a production time ratio of a basic voltage vector has a minimum value that depends on a magnitude of

25 the bus voltage Vdc and a limitation on a hardware side of the inverter main circuit 1 and the like.
[0117]

Thus, since a sum of three-phase currents is zero, when this fact is utilized, control of the motor 7 is

30 established if current information of at least two phases is obtained. Taking notice of this, the third embodiment makes it possible to secure an operation range on the low speed side of the motor 7. Specifically, if a production

time ratio, which is allocated to a voltage vector in the middle among three kinds of basic voltage vectors having phase differences of 60 degrees, is set to a predetermined value such as a minimum value, it is possible to secure

5   production time ratios, which make it possible to detect an electric current, in two basic voltage vectors having a phase difference of 120 degrees on both sides of the voltage vector in the middle. Thus, even in such a special range, it is possible to continue to control the motor 7.

10 Note that, when the minimum value is adopted as the predetermined value, a lower limit of a generation maintenance time of PWM depends on a semiconductor switching element or a CPU for calculating the generation maintenance time. Thus, the minimum value of the

15 production time ratio is determined taking into account a limit of hardware.

[0118]

This is explained specifically with reference to Figs. 28A to 28C. Fig. 28A has the same content as Fig. 2A and

20 is a diagram for explaining an operation of the PWM-signal-duty creating unit 22. Fig. 28B corresponds to Fig. 2B and is a diagram for explaining a virtual voltage vector used in the PWM-signal-duty redistributing unit 23 according to the third embodiment. Fig. 28C corresponds to Fig. 2C and

25 is a diagram for explaining an operation of the PWM-signal-duty redistributing unit 23 according to the third embodiment.

[0119]

In Fig. 28A, basic voltage vectors V3 and V2 are

30 arranged at an interval of 60 degrees clockwise on a phase plane having a direction of the basic voltage vector V1 as an initial phase. When an inverter rotation angle θ is near 60 degrees, that is, when the voltage command vector

V* is near the basic voltage vector V3 (in Fig. 2A, the voltage command vector V* is near the basic voltage vector V3). A state of generation of production time ratios in this case is shown in Fig. 28A. As shown in Fig. 28A, when the voltage command vector V* is present between the basic voltage vector V1 and the basic voltage vector V3, the PWM-signal-duty creating unit 22 decomposes the voltage command vector V* in two directions of the basic voltage vector V1 and the basic voltage vector V3 to thereby generate a production time ratio d1 of the basic voltage vector V1 and a production time ratio d3 of the basic voltage vector V3.

[0120]

In Fig. 28B, three virtual voltage vectors 30, 31, and 32 with phase differences of 120 degrees having equal production time ratios d' are superimposed on three basic voltage vectors V1, V3, and V2 shown in Fig. 28A. As shown in Fig. 28B, the virtual voltage vector 30 is in-phase with the basic voltage vector V1, the virtual voltage vector 31 is anti-phase with the basic voltage vector V3, and the virtual voltage vector 32 is in-phase with the basis voltage vector V2.

[0121]

The PWM-signal-duty redistributing unit 23 according to the third embodiment superimposes three virtual voltage vectors in directions of basic voltage vectors having phase differences of 120 degrees, respectively, to add up production time ratios of both the virtual voltage vectors and the basic voltage vectors such that a direction of a basic voltage vector, which has a short production time ratio and with which current detection is difficult, is included. The minimum value dmin described above is given as a production time ratio of the basic voltage vector in the middle. In the example shown in Fig. 28A, since the

basic voltage vectors V1 and V2 are two basic voltage vectors on both sides and the basic voltage vector V3 is the basic voltage vector in the middle, as shown in Fig. 28C, the PWM-signal-duty redistributing unit 23 adds up

5   production time ratios of the basic voltage vector V1 and the basic voltage vector V2 and the virtual voltage vectors corresponding to the basic voltage vectors among the three virtual voltage vectors with the equal production time ratios d'. However, the PWM-signal-duty redistributing

10   unit 23 gives the minimum value dmin as a production time ratio of the basic voltage vector V3 in the middle.
[0122]

A relation between the minimum value dmin and the production time ratio d3 of the basic voltage vector V3

15   calculated in Fig. 28A is dmin=d3-d'. Therefore, the production time ratios d' of the virtual voltage vectors, that is, lengths of the virtual voltage vectors only have to be set as d'=d3-dmin to satisfy this Equation. Note that the production time ratios d1' and d2' in the

20   directions of the basic voltage vectors V1 and V2 are d1'=d1+d' and d2'=d' as explained with reference to Fig. 2C.
[0123]

However, a production time ratio given to a basic voltage vector in the middle at the time when basic voltage

25   vectors are redistributed does not always have to be the minimum value dmin. The production time ratio only has to be set to a predetermined value according to a type of the motor 7 used and a condition on a load side. The predetermined value given as the production time ratio of

30   the basic voltage vector in the middle may be changed according to an operation frequency or the like as required.
[0124]

A production time ratio according to the third

embodiment is explained in comparison with the conventional system to show that the third embodiment has an advantage. Fig. 29A is a graph of production time ratios of two kinds of basic voltage vectors and a zero vector at a percentage modulation 0.3 obtained in the conventional three-phase modulation system or two-phase modulation system. Fig. 29B is a graph of production time ratios of three kinds of basic voltage vectors and a zero vector at a percentage modulation 0.3 obtained in the third embodiment. Note that, in Fig. 29B, the minimum value dmin is set to 4%. In Figs. 29A and 29B, basic voltage vectors are a basic voltage vector 1, a basic voltage vector 2, and a basic voltage vector 3 in an order of appearance in an inverter rotation direction.

[0125]

As it can be understood from comparison of Figs. 29A and 29B, in the method of generating a PWM signal according to the third embodiment, production time ratios of the two basic voltage vectors on both sides can be secured more regardless of an inverter rotation angle. In the conventional method shown in Fig. 29A, controllability of the motor 7 is deteriorated as a percentage modulation falls. Thus, it is also evident from the figure that the method shown in the third embodiment is effective.

[0126]

The above description is about the method according to the first embodiment, that is, the method of using one kind of a zero vector. In the method according to the second embodiment, that is, the method of using two kinds of zero vectors, since a total production time ratio of the zero vectors are the same, operation performance is not affected and it is possible to generate a PWM waveform with a high vibration/noise reduction effect.

[0127]

When two kinds of zero vectors are used, to secure an operation range on the low speed side of the motor 7, if it is desired to make the motor 7 controllable even if a percentage modulation is set lower, that is, if it is desired to make the motor 7 controllable even if a vector length |V*| of the voltage command vector V* is set shorter, as described above, a production time ratio only has to be set to the predetermined value (the minimum value dmin) for a vector in the middle among three kinds of basic voltage vectors having phase differences of 60 degrees. Consequently, it is possible to secure a production time ratio that makes it possible to detect an electric current with two basic voltage vectors having a phase difference of 120 degrees on both sides of the voltage command vector V*. This makes it possible to continue to control the motor 7. A production time ratio of a vector in the middle in redistributing basic voltage vectors does not always have to take the minimum value dmin and only has to be set to a predetermined value according to a type of the motor 7 used and a condition on a load side. The minimum value dmin ma be changed according to an operation frequency or the like as required.

[0128]

As descried above, according to the third embodiment, a length of a basic voltage vector in the middle among three kinds of basic voltage vectors having phase differences of 60 degrees is set to a predetermined value such that production time ratios of the two kinds of basic voltage vectors on both sides can be secured regardless of an inverter rotation angle. Thus, it is possible to increase an operation range on a low speed side of a motor.

[0129]

Fourth embodiment

Figs. 30A to 30C are graphs for explaining, in an inverter including a three-phase PWM-signal generating apparatus according to a fourth embodiment of the present invention, an operation of a PWM-signal generating unit in the three-phase PWM-signal generating apparatus. In the fourth embodiment, an operation request range on a low speed side is stricter than that in the third embodiment. In other words, a percentage modulation is lower than that in the third embodiment and, when a voltage command vector is decomposed into vectors in two directions, both production time ratios of the vectors in the two directions are short. An example of a constitution explained the fourth embodiment copes with this case.

[0130]

According to the fourth embodiment, in the PWM-signal creating unit 21 in the constitution shown in Fig. 1 (the first embodiment), the PWM-signal-duty creating unit 22 performs the same operation as the first embodiment. However, the PWM-signal-duty redistributing unit 23 performs an operation from the operation in the third embodiment. The fourth embodiment is explained below with reference to Figs. 30A to 30C.

[0131]

Fig. 30A has the same content as Figs. 2A and 16A and is a diagram for explaining an operation of the PWM-signal-duty creating unit 22. Fig. 30B corresponds to Figs. 2B and 16B and is a diagram for explaining virtual voltage vectors used in the PWM-signal-duty redistributing unit 23 according to the fourth embodiment. Fig. 30C corresponds to Figs. 2C and 16B and is a diagram for explaining an operation of the PWM-signal-duty redistributing unit 23 according to the fourth embodiment.

[0132]

In Fig. 30A, basic voltage vectors V3 and V2 are arranged at an interval of 60 degrees clockwise on a phase plane having a direction of the basic voltage vector V1 as an initial phase. When the inverter rotation angle θ is in an area of 30 to 60 degrees on the phase plane, a magnitude of the voltage command vector V* present between the basic voltage vectors V1 and V3 is short. A state of generation of production time ratios in this case is shown in Fig. 30A. In this case, as in Figs. 2A and 16A, the PWM-signal-duty creating unit 22 decomposes the voltage command vector V* in two directions of the basic voltage vector V1 and the basic voltage vector V3 to thereby generate a production time ratio d1 of the basic voltage vector V1 and a production time ratio d3 of the basic voltage vector V3.

[0133]

However, in the example shown in Fig. 30A, since both the production time ratio d1 of the basic voltage vector V1 and the production time ratio d3 of the basic voltage vector V3 are low, it is difficult to detect an electric current when the basic voltage vectors V1 and V3 are produced. Thus, as in the third embodiment, the PWM-signal-duty redistributing unit 23 carries out processing for adding virtual voltage vectors (Figs. 30B and 30C).

[0134]

In Fig. 30B, three virtual voltage vectors 35C6, and 37 with phase differences of 120 degrees having equal production time ratios d' are superimposed on three basic voltage vectors V1, V3, and V2 having phase differences of 60 degrees shown in Fig. 30A. As shown in Fig. 30B, the virtual voltage vector 35 is in-phase with the basic voltage vector V1, the virtual voltage vector 36 is anti-phase with the basic voltage vector V3, and the virtual

voltage vector 37 is in-phase with the basis voltage vector V2.

[0135]

In the third embodiment (Fig. 16C), the production time ratios d1', d2', and d3' of the basic voltage vectors V1, V2, and V3 are represented as d1'=d1+d', d2'=d', and d3'=d3-d'. The production time ratio d3' has positive polarity. On the other hand, in the fourth embodiment, the PWM-signal-duty redistributing unit 23 superimposes three virtual voltage vectors having the equal production time ratios d' in directions of the basic voltage vectors V1, V2, and V4 (-V3) having phase differences of 120 degrees to add up production time ratios thereof such that the production time ratio d3' has a negative polarity. Production time ratios obtained as a result of the addition are d1', d2', and d4' as shown in Fig. 30C. Production time ratios d1', d2', and d4' in this case are represented as d1'=d1+d', d2'=d', and d4'=d'-d3.

[0136]

A constraint in this case is that a result of addition does not exceed a value 1. In other words, d1'+d2'+d4'≤1 is a constraint in the PWM-signal-duty redistributing unit 23. It is possible to perform vector redistribution within this range. In other words, in the control system according to the fourth embodiment, unlike the third embodiment, a production time ratio of the voltage command vector V* is redistributed to three kinds of basic voltage vectors having phase differences of 120 degrees and one kind of a zero vector.

[0137]

Since a percentage modulation is a ratio of an output voltage to a bus voltage, the bus voltage increases and the percentage modulation falls as operation speed is lower and

a load is lighter. Therefore, when the magnitudes d' of virtual vectors are set in the same manner as the third embodiment, polarities of the production time ratios d3' and d4' obtained in the processing for addition with the

5 virtual vectors are decided according to a degree of lowness of the percentage modulation. Thus, it is decided which of the basic voltage vector V3 and the basic voltage vector V4 is used by monitoring the polarities of the production time ratios d3' and d4'. In other words, as a

10 result of the monitoring, if a production time ratio in a positive value is d3', the basic voltage vector V3 is used and the control system according to the third embodiment is adopted. If a production time ratio in a positive value is d4', the basic voltage vector V4 is used and the control

15 system according to the fourth embodiment is adopted.
[0138]

In other words, it is possible to switch a control system to be adopted by managing the magnitudes d' of virtual vectors. When a low speed operation request range

20 is not strict, even if a degree of lowness of the percentage modulation is "large", the control system according to the third embodiment is adopted. When a low speed operation request range is strict, even if a degree of lowness of the percentage modulation is "small", the

25 control system according to the fourth embodiment is adopted.
[0139]

Specifically, when a low speed operation request range is not strict, the magnitudes d' of virtual vectors are

30 managed to set the production time ratio d3' to a positive polarity or set the production time ratio D4' to a negative polarity, that is, not to produce a basic voltage vector in the direction of the basic voltage vector V4. On the other

hand, when a low speed operation request range is strict, as shown in Fig. 30C, the magnitudes d' of virtual vectors are managed to produce a basic voltage vector in the direction of the basic voltage vector V4.

5　[0140]

A three-phase PWM signal, which is generated when the percentage modulation according to the fourth embodiment is extremely low, is explained specifically with reference to Figs. 31A to 34B. Figs. 31A and 31B are diagrams of a relation on a phase plane at the time when an inverter rotation angle is near 60 degrees in generating a PWM signal using three kinds of basic voltage vectors having phase differences of 120 degrees and one kind of a zero vector and an example of an order of switching of the three kinds of basic voltage vectors having phase differences of 120 degrees and the one kind of a zero vector (a pattern #31). Figs. 32A and 32B are timing charts of a logical state (a switching pattern) of semiconductor switching elements on a DC bus positive pole side controlled according to two ways of the switching of the three kinds of basic voltage vectors having phase differences of 120 degrees and the one kind of a zero vector shown in Fig. 31B. Figs. 33A and 33B are diagrams of a relation on a phase plane at the time when an inverter rotation angle is near 120 degrees in generating a PWM signal using three kinds of basic voltage vectors having phase differences of 120 degrees and one kind of a zero vector and an example of an order of switching of the three kinds of basic voltage vectors having phase differences of 120 degrees and the one kind of a zero vector (a pattern #32). Figs. 34A and 34B are timing charts of a logical state (a switching pattern) of semiconductor switching elements on a DC bus positive pole side controlled according to two ways of the switching

of the three kinds of basic voltage vectors having phase differences of 120 degrees and the one kind of a zero vector shown in Fig. 33B.

[0141]

5   In Fig. 31A, the basic voltage vector V1 (0, 0, 1), the basic voltage vector V2 (0, 1, 0), the basic voltage vector V4 (1, 0, 0), and the zero vector V0 (0, 0, 0), which relate to one another when the inverter rotation angle θ is near 60 degrees (in the direction of the basic

10   voltage vector V6) with the basic voltage vector V1 as an initial phase, are shown. In Fig. 31B, as a switching order in this case (the pattern #31), for example, two ways of switching, (a) V0, V1, V0, V2, V0, and V4 and (b) V0, V1, V0, V4, V0, and V2, are shown. Note that the switching

15   orders (a) and (b) shown in Fig. 31B may be reversed. Specifically, in the example of the switching order (a), the switching order may be V4, V0, V2, V0, V1, and V0. Figs. 32A and 32B show logical states (switching patterns) during one carrier control period of the semiconductor

20   switching elements 5a, 5c, and 5e on a DC bus positive pole side in the switching orders (a) and (b) shown in Fig. 31B.

[0142]

       The pattern #31 described above is applied when the inverter rotation angle θ is near 100 degrees (in the

25   direction of the basic voltage vector V2) and when the inverter rotation angle θ is near 300 degrees (in the direction of the basic voltage vector V5).

[0143]

       When the example of Fig. 30C is applied to Figs. 32A

30   and 32B, a conducting time ratio of the U-phase positive pole side switching element is d1'. A conducting time ratio of the V-phase positive pole side switching element

is d2'. A conducting time ratio of the W-phase positive pole side switching element is d4'. Conducting time ratios of negative pole side switching elements in the respective phases are calculated by subtracting the conducting time ratios of the positive pole side switching elements from the value 1. Conducting times during one carrier control period of the respective switching elements are decided by multiplying these values by one carrier control period. At the time of actual PWM signal output, a PWM signal is generated taking into account a short circuit prevention time of a switching element.

[0144]

In this way, the PWM-signal-duty redistributing unit 23 shown in Fig. 1 obtains the conducting times Tup, Tvp, and Twp during one carrier control period of the U-phase, V-phase, and W-phase positive pole side switching elements and the conducting times Tun, Tvn, and Twn during one carrier control period of the negative pole side switching elements. Based on the conducting times, the PWM-signal generating unit 15 emits driving signals Up, Vp, Wp, Un, Vn, and Wn to the semiconductor switching elements 5a, 5c, 5e, 5b, 5d, and 5f to make it possible to drive the motor 7.

[0145]

In Fig. 33A, the basic voltage vector V3 (0, 1, 1), the basic voltage vector V6 (1, 1, 0), the basic voltage vector V5 (1, 0, 1), and the zero vector V7 (1, 1, 1), which relate to one another when the inverter rotation angle θ is near 120 degrees (in the direction of the basic voltage vector V2) with the basic voltage vector V1 as an initial phase, are shown. In Fig. 33B, as a switching order in this case (the pattern #32), for example, two ways of switching, (a) V7, V3, V7, V6, V7, and V5 and (b) V7, V3, V7, V5, V7, and V6, are shown. Note that the switching

orders (a) and (b) shown in Fig. 33B may be reversed. Specifically, in the example of the switching order (a), the switching order may be V5, V7, V6, V7, V3, and V7. Figs. 34A and 34B show logical states (switching patterns) during one carrier control period of the semiconductor switching elements 5a, 5c, and 5e on a DC bus positive pole side in the switching orders (a) and (b) shown in Fig. 33B.

[0146]

Since a correspondence relation between Figs. 33A and 33B and with Fig. 30C can be explained as described above, the correspondence relation is not described again. The pattern #32 described above is applied when the inverter rotation angle θ is near 240 degrees (in the direction of the basic voltage vector V4) and when the inverter rotation angle θ is near 0 degree (in the direction of the basic voltage vector V). In the same idea as explained in the first embodiment, it is possible to switch the method of generating a PWM signal according to the inverter rotation angle θ using the switching phase angle $\theta\alpha$.

[0147]

As described above, according to the fourth embodiment, when a voltage command vector is smaller than that in the third embodiment, a PWM signal is generated using three kinds of basic voltage vectors having phase differences of 120 degrees and one kind of a zero vector. Thus, it is possible to detect an electric current surely even when a percentage modulation is extremely low.

[0148]

It is possible to switch and apply the control system according to the third embodiment and the control system according to the fourth embodiment according to whether an operation request range on a low speed side is strict.

Thus, a three-phase voltage inverter more excellent in convenience of use is obtained.

[0149]

In the explanation of the fourth embodiment, three kinds of basic voltage vectors having phase differences of 120 degrees and one kind of a zero vector are used. However, as in the second and the third embodiments, it is possible to generate a PWM signal in the same idea when two kinds of zero vectors are used. The method of distributing a zero vector into two is explained in the second and the third embodiment. Thus, an explanation of the method is omitted.

[0150]

Fifth embodiment

Figs. 35A to 35C are graphs for explaining, as a fifth embodiment of the present invention, a method of constitution at the time when both the method of generating a PWM signal according to the first to the fourth embodiments explained above and the method of generating a PWM signal according to the conventional three-phase modulation system or two-phase modulation system are used. The PWM-signal creating unit 21 shown in Fig. 1 has a constitution in which the PWM-signal-duty redistributing unit 23 is added to the PWM duty producing unit 22 equivalent to the PWM-signal creating unit 14 shown in Fig. 36. Thus, it is possible to use both the methods.

[0151]

As shown in Fig. 35A, in a characteristic of relation between an operation frequency and a load torque of a motor, for example, it is possible to adopt a constitution for setting a switching point 41 before shift to high speed operation, generating a PWM signal according to the first and the second embodiment with the PWM-signal creating unit

21 shown in Fig. 1 at low speed, and generating a PWM
signal according to the conventional three-phase modulation
system or two-phase modulation system with the PWM-signal
creating unit 14 shown in Fig. 36 at high speed. When
5   switching is performed according to an actual operation
frequency, it is possible to prevent an adverse effect like
hutching by giving a hysteresis characteristic to a
switching frequency. Note that the operation frequency may
be an actual operation frequency or may be an operation
10 frequency command. According to this constitution, it is
possible to optimize efficiency and reduce processing loads
of a CPU or the like in a high speed operation area.
[0152]

As shown in Fig. 35B, in a characteristic of relation
15 between an operation frequency and a load torque of a motor,
for example, it is possible to adopt a constitution for
setting a switching point 42 to a predetermined value of a
load torque applied to the motor indicating a high load or
a predetermined value of an electric current flowing to the
20 motor indicating a high current, generating a PWM signal
according to the first and the second embodiments with the
PWM-signal creating unit 21 shown in Fig. 1 when a light
load or a low current is observed, and generating a PWM
signal according to the conventional three-phase modulation
25 system or two-phase modulation system with the PWM-signal
creating unit 14 shown in Fig. 36 when a high load or a
high current is observed. In this case, it is also
possible to prevent an adverse effect like hutching by
giving a hysteresis characteristic to a threshold.
30 According to this constitution, it is possible to optimize
efficiency and reduce processing loads of a CPU or the like
in a high speed operation area.
[0153]

In Fig. 35C, an example in which a method of
generating a PWM signal is switched according to an
inverter rotation angle is shown. It is possible to adopt
a constitution for setting switching points in respective
5   ranges such that a PWM signal is generated as described
below. For example, when the inverter rotation angle is in
ranges of 15 degrees to 45 degrees, 75 degrees to 105
degrees, 135 degrees to 165 degrees, 195 degrees to 225
degrees, 255 degrees to 285 degrees, and 315 degrees to 345
10 degrees on a phase plane, the PWM-signal creating unit 14
shown in Fig. 36 produces a PWM signal according to the
conventional three-phase modulation system or two-phase
modulation system. In the other ranges of 0 degree to 15
degrees, 45 degrees to 75 degrees, 105 degrees to 135
15 degrees, 165 degrees to 195 degrees, 225 degrees to 255
degrees, 285 degrees to 315 degrees, and 345 degrees to 360
degrees, the PWM-signal creating unit 21 shown in Fig. 1
generates a PWM signal in the system according to the first
to the fourth embodiments. In this way, the two PWM signal
20 generating methods are used properly when a voltage command
vector is passing near directions of respective basic
voltage vectors and when a voltage command vector is
passing through the other areas. This makes it possible to
optimize efficiency in, in particular, a low speed
25 operation area.
[0154]

Note that the switching points shown in Fig. 35C can
be set as fixed values according to an inverter rotation
angles. However, the switching points may be arbitrary
30 values determined according to a short circuit prevention
time of inverter switching elements, a noise generation
amount depending on hardware, an AD value detection time
depending on a CPU, a percentage modulation at the time of

operation of a motor, or the like. It is also possible to switch the modulation methods according to an operation frequency, a magnitude of a load torque, a percentage modulation, an electrical angle, or the like. Since it is

5   possible to optimize efficiency by using a plurality of PWM signal generating methods in combination as required, a higher vibration/noise reduction effect is obtained.

[0155]

As explained above, according to the first to the

10   fifth embodiments, a three-phase PWM signal is generated using three kinds of actual vectors and one kind or two kinds of zero vectors. Thus, even in an area where a percentage modulation is low or, for example, when an inverter rotation angle at the time when a direction of the

15   basic voltage vector V1 is set as an initial phase is near integer times of 60 degrees or 30 degrees, it is possible to perform detection of a DC bus current accurately. In particular, it is possible to improve controllability even at the time of a low load operation and a low speed

20   operation.

[0156]

It is also possible to reduce deterioration of efficiency. It is also possible to reduce an influence on noise and vibration. It is possible to use the method in a

25   range where a percentage modulation is high. In addition, since a PWM signal is generated based on the conventional three-phase modulation system or two-phase modulation system, an influence on a load of software is little. Thus, it is possible to switch a modulation system to the three-

30   phase modulation system or the two-phase modulation system easily when switching of the modulation system is necessary. It is possible to improve reliability for startup. It is possible to apply the method to a three-phase induction

motor or a synchronous motor.

[0157]

In particular, when a three-phase PWM signal is generated using three kinds of actual vectors and two kinds of zero vectors, a noise reduction effect near a carrier frequency is obtained more easily than using three kinds of actual vectors and one kind of a zero vector.

INDUSTRIAL APPLICABILITY

[0158]

As described above, the three-phase PWM-signal generating apparatus according to the present invention is useful for expanding a range of application of the three-phase voltage inverter.